ES8327

Low Power Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I^2S/PCM/TDM master or slave serial data port
- 256/384Fs, USB 12/24 MHz and other non standard audio system clocks
- I^2C interface

Stereo DMIC

- Support 2-ch digital microphone
- 24-bit, 8 to 96 kHz sampling frequency
- 110 dB signal to noise ratio, -100 dB THD+N

Mono ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 102 dB signal to noise ratio, -90 dB THD+N
- Two pairs of analog input with differential input option
- Low noise pre-amplifier
- Auto level control (ALC) and noise gate
- Noise reduction filter

Stereo DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 100 dB signal to noise ratio, -85 dB THD+N
- Ground centered headphone driver
- Dynamic range compression
- Headset detection
- OMTP and CTIA auto switch
- Pop and click noise suppression

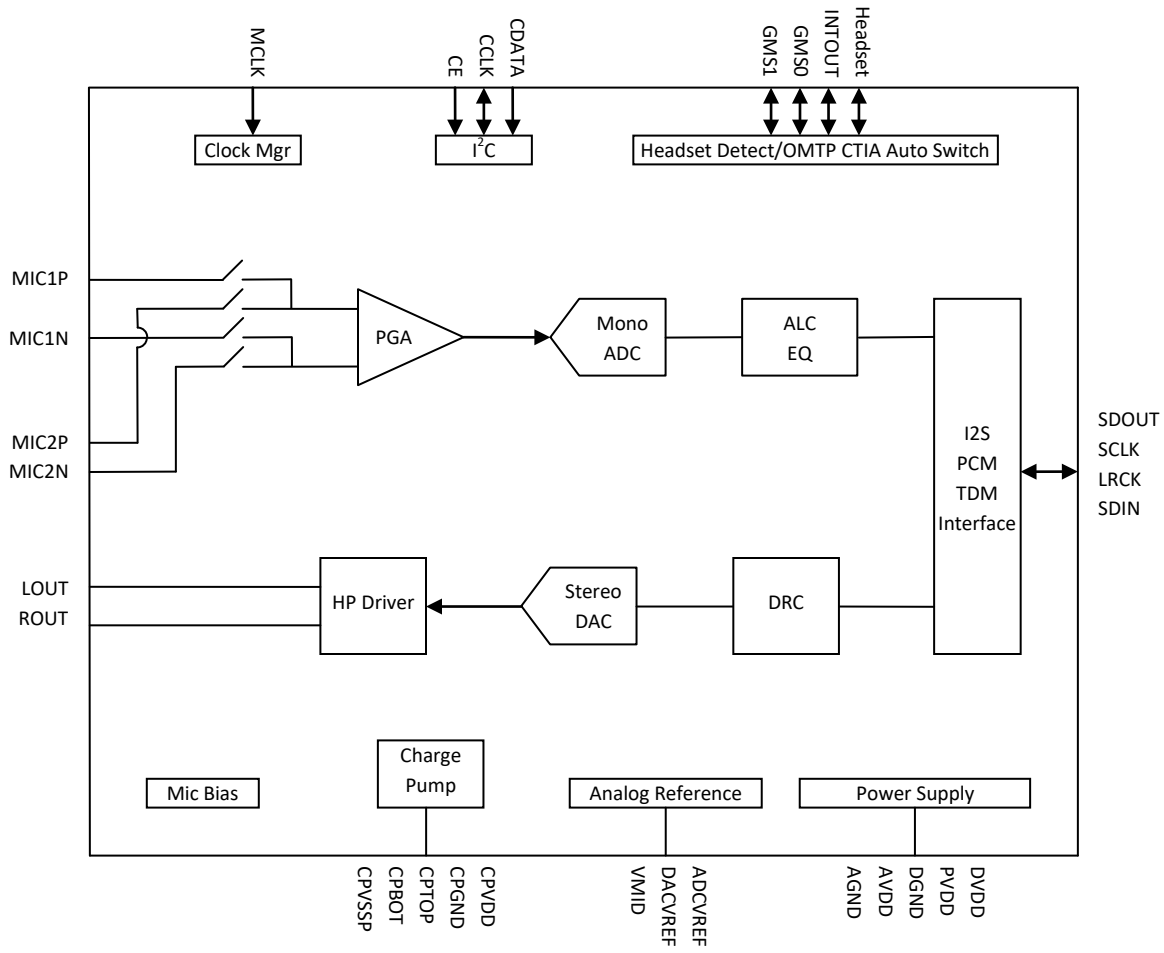
APPLICATIONS

- Notebook
- Tablet
- PC

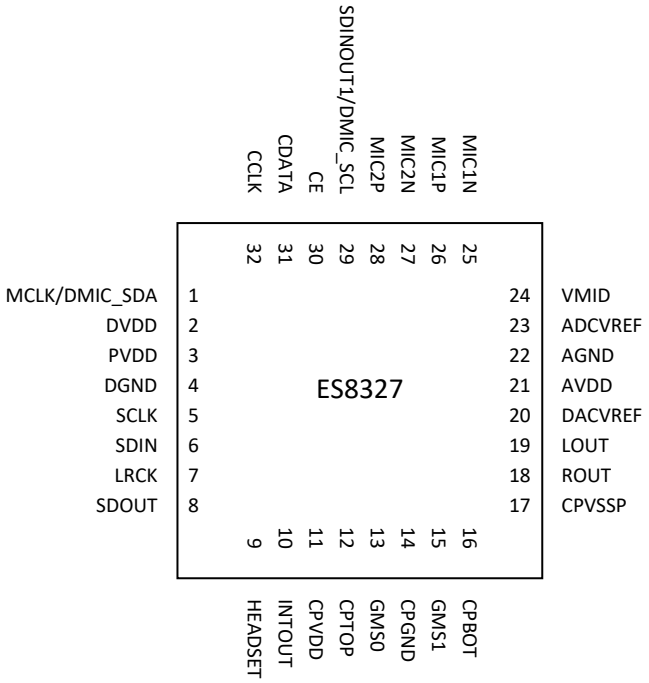
ORDERING INFORMATION

ES8327 -40°C ~ +85°C
QFN-32

1. BLOCK DIAGRAM

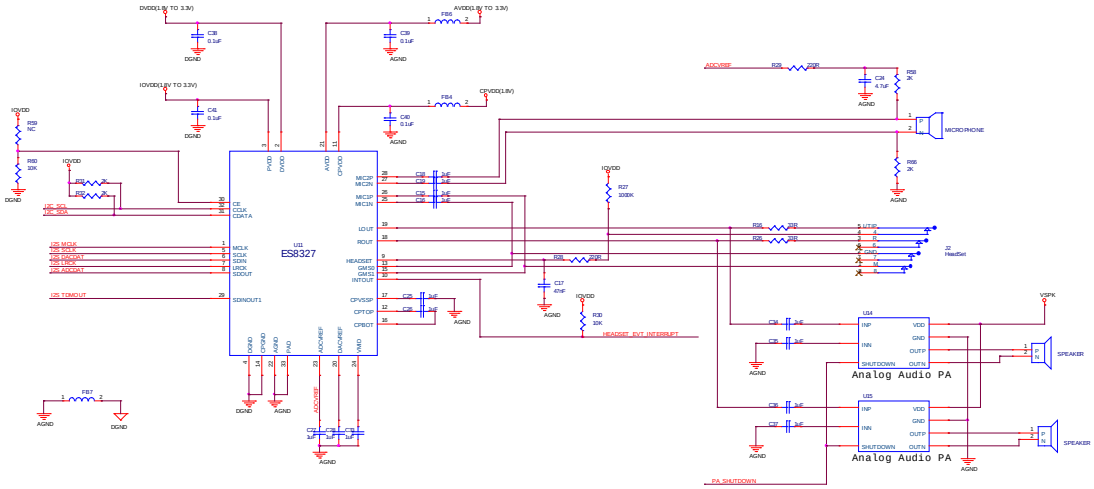


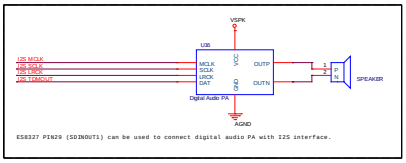
2. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA, CE	32, 31, 30	I, I/O, I	I^2C clock, data, address
MCLK/DMIC_SDA	1	I	Master clock or DMIC input
SCLK	5	I/O	Serial data bit clock
SDIN	6	I	DAC serial data input
LRCK	7	I/O	Serial data left and right channel frame clock
SDOUT	8	O	ADC serial data output
SDINOUT1/DMIC_SCL	29	O	SDOUT1 from SDIN (TDM) or DMIC bit clock
MIC2P MIC2N	28 27	I	Analog mic 2 input P Analog mic 2 input N
MIC1P MIC1N	26 25	I	Analog mic 1 input P Analog mic 1 input N
HEADSET, INTOUT GMS0, GMS1	9, 10 13, 15	I/O	Headset detect and interrupt OMTP and CTIA auto switch
LOUT, ROUT	19, 18	O	DAC stereo analog output
PVDD	3	Analog	Power supply for the digital input and output
DVDD, DGND	2, 4	Analog	Digital power supply
AVDD, AGND	21, 22	Analog	Analog power supply
CPVDD, CPGND	11, 14	Analog	Charge pump power supply
CPTOP, CPBOT	12, 16	Analog	Charge pump capacitor top and bottom
CPVSSP	17	Analog	Charge pump filtering capacitor connection
VMID	24	Analog	Filtering capacitor connection
ADCVREF, DACVREF	23, 20	Analog	Filtering capacitor connection

3. TYPICAL APPLICATION CIRCUIT





IOVDD	IO Power Supply, 1.8V to 3.3V. Please refer to ES8327 Datasheet
DVDD	Digital Power Supply, 1.8V to 3.3V. Please refer to ES8327 Datasheet
AVDD	Analog Power Supply, 1.8V to 3.3V. Please refer to ES8327 Datasheet
CPVDD	Charge Pump Power Supply, must be 1.8V. One 1.8V LDO is recommended for CPVDD power supply Please refer to ES8327 Datasheet

CE	I2C Chip Address.	pulled up to PVDD, I2C Chip Address = 0x19
		pulled down to GND, I2C Chip Address = 0x18
HEADSET_EVT_INTERRUPT	An Interrupt Signal to Host SOC / CPU	
ADCVREF	ADCVREF can be used as Microphone Power Supply.	

4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (32Fs, 64Fs, 128Fs, 256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (16 MHz, 25 MHz, 26 MHz, etc).

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 0011 00x, where x equals CE. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I²C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0011 00 CE	0	ACK	RAM	ACK	DATA	ACK	Stop

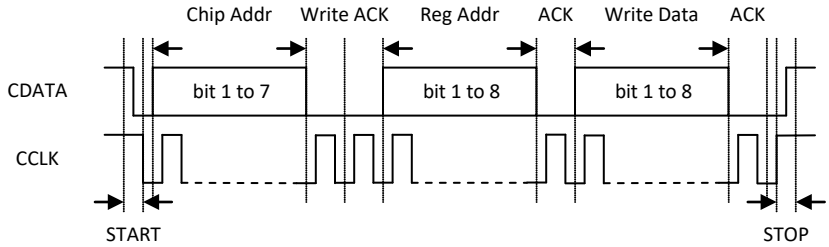


Figure 1a I²C Write Timing

Table 2 Read Data from Register in I²C Interface Mode

	Chip Address	R/W		Register Address		
Start	0011 00 CE	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0011 00 CE	1	ACK	Data	NACK	Stop

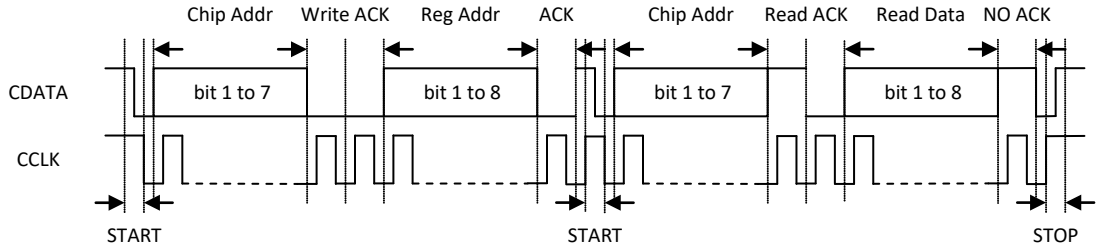


Figure 1b I²C Read Timing

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and SDIN or SDOUT pins. These formats are I^2S, left justified, DSP/PCM and TDM. DAC input SDIN is sampled by the device on the rising edge of SCLK. ADC data is out at SDOUT on the falling edge of SCLK. The relationship of SDATA (SDIN/SDOUT), SCLK and LRCK with these formats are shown through Figure 2a to Figure 2h.

SDIN 6-ch TDM data can directly output to 2-ch SDINOUT1, 2-ch SDINOUT2 and 2-ch SDINOUT3.

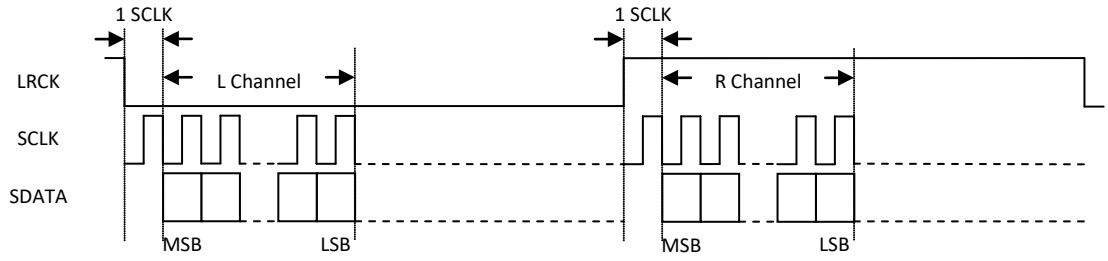


Figure 2a I^2S Serial Audio Data Format

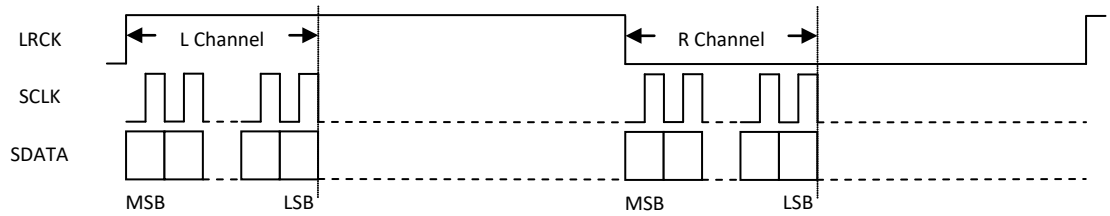


Figure 2b Left Justified Serial Audio Data Format

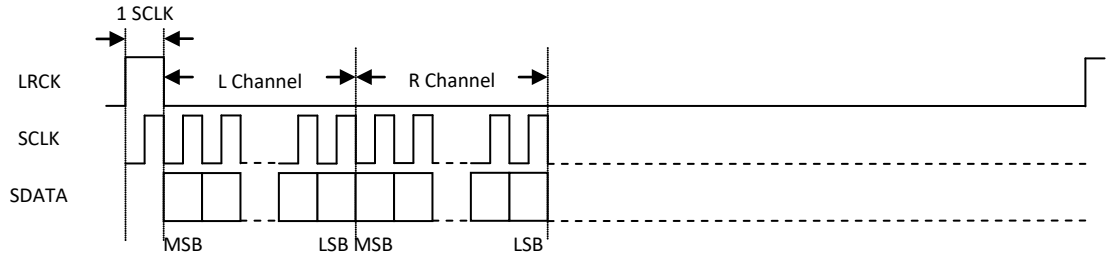


Figure 2c DSP/PCM Mode A Serial Audio Data Format

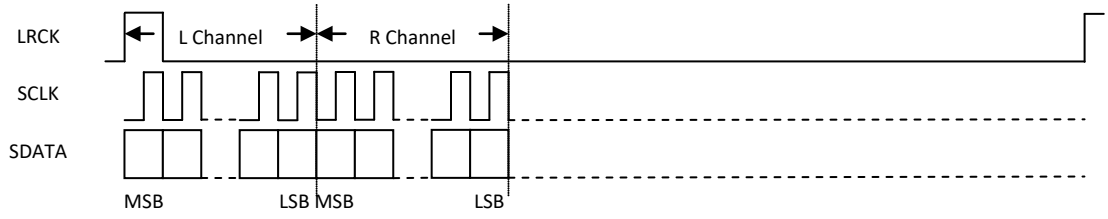


Figure 2d DSP/PCM Mode B Serial Audio Data Format

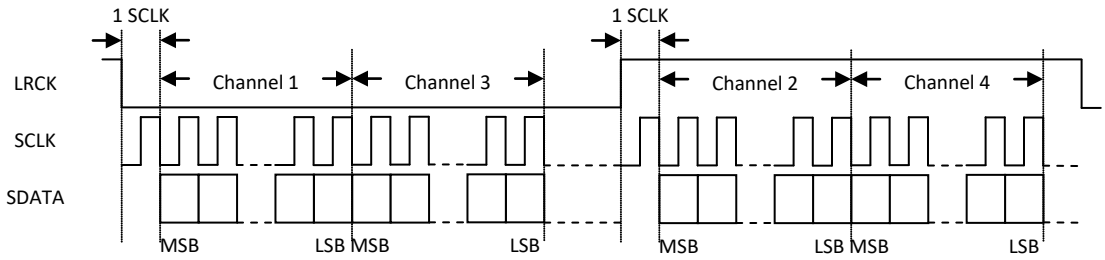


Figure 2e TDM I^{2}S Serial Audio Data Format

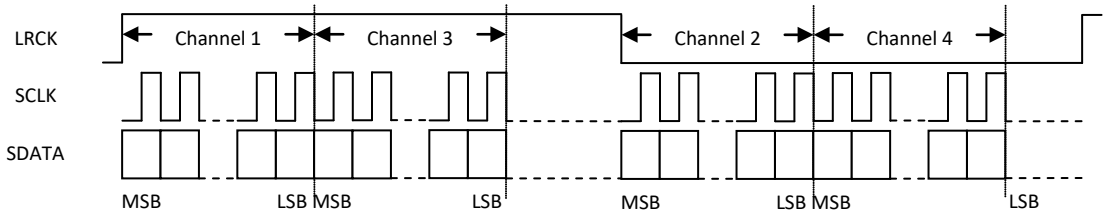


Figure 2f TDM Left Justified Serial Audio Data Format

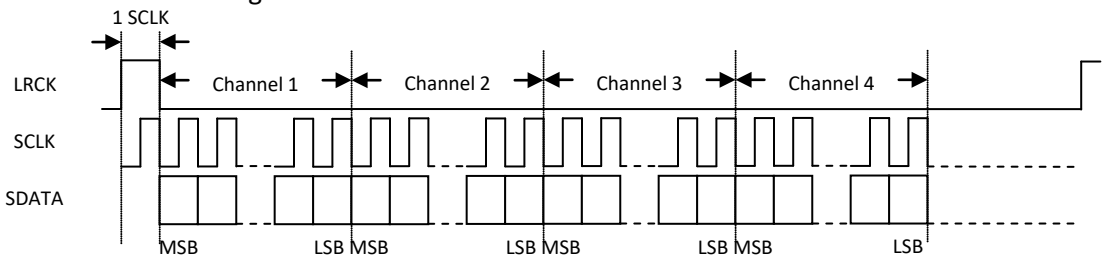


Figure 2g TDM DSP/PCM Mode A Serial Audio Data Format

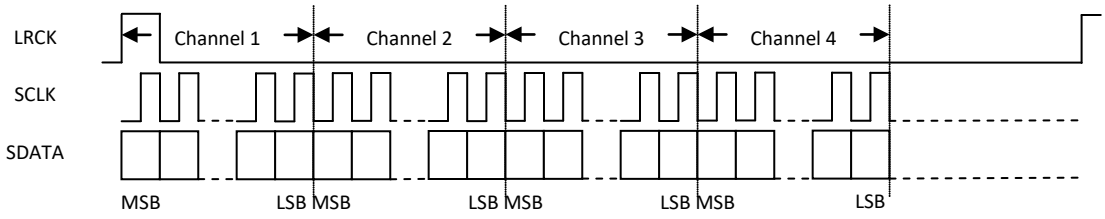


Figure 2h TDM DSP/PCM Mode B Serial Audio Data Format

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+105°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
AVDD	1.7	1.8/3.3	3.6	V
CPVDD (Note 1)	1.6	1.8	2.0	V
DVDD (Note 2)	1.6	1.8/3.3	3.6	V
PVDD	1.6	1.8/3.3	3.6	V

Note 1: recommend an option to add a LDO in PCB for CPVDD, in case CPVDD supply is noisy.

Note 2: DVDD 3.3V (±10%) support up to 96 kHz; DVDD 1.8V (±10%) support up to 24 kHz or up to 48 kHz with 256Fs or 512Fs MCLK.

Note 3: recommend all power supply turn on or off within 10 ms of each other.

Note 4: recommend all power supply on, entering low power through control register setting, then stopping input clock.

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	97	102	104	dB
THD+N	-93	-90	-87	dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input (differential P and N)		AVDD/3.3		Vrms
Input Impedance		6		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	95	100	102	dB
THD+N	-88	-85	-82	dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Analog Output				
Full Scale Output Level		AVDD/3.3		Vrms

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V DVDD=1.8V, PVDD=1.8V, AVDD=1.8V		TBD		mW
Power Down Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V DVDD=1.8V, PVDD=1.8V, AVDD=1.8V		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER		Symbol	MIN	MAX	UNIT
MCLK frequency				49.2	MHz
MCLK duty cycle			40	60	%
LRCK frequency				100	KHz
LRCK duty cycle (Note 5)			40	60	%
SCLK frequency				26	MHz
SCLK pulse width low		T_{SLKL}	16		ns
SCLK Pulse width high		T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)		T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)		T_{LSR}	10		ns
SCLK falling to SDOUT valid	VDDD=3.3V VDDD=1.8V	T_{SDO}		16 39	ns
LRCK edge to SDOUT valid (Note 6)	VDDD=3.3V VDDD=1.8V	T_{LDO}		11 25	ns

SDIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to SDIN hold time	T_{SDIH}	10		ns

Note 5: one SCLK period of high time in DSP/PCM modes.

Note 6: only apply to MSB of Left Justified or DSP/PCM mode B.

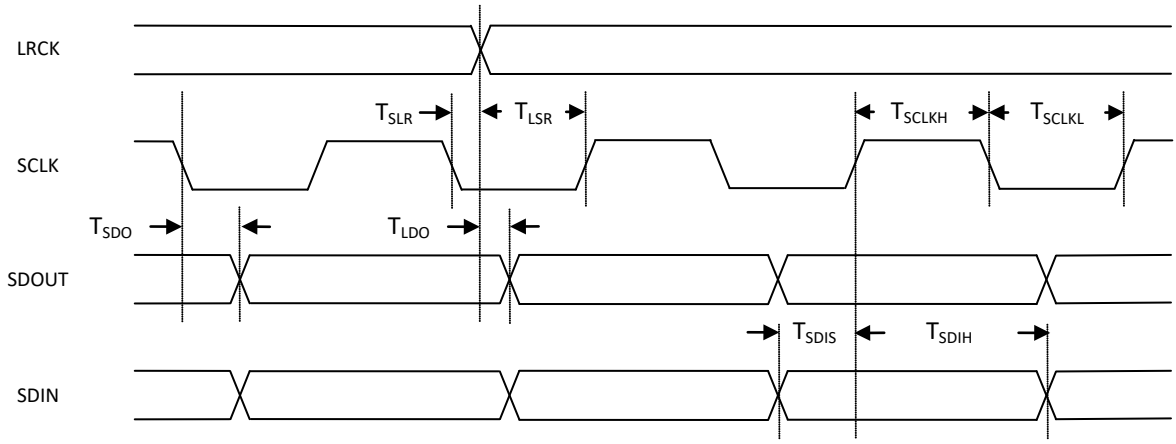


Figure 3 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

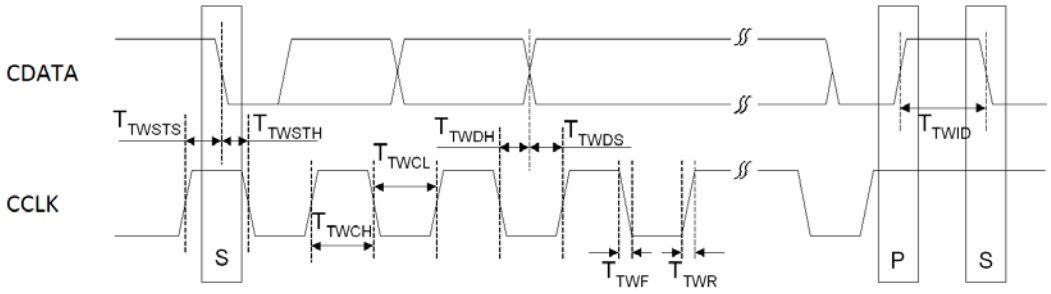
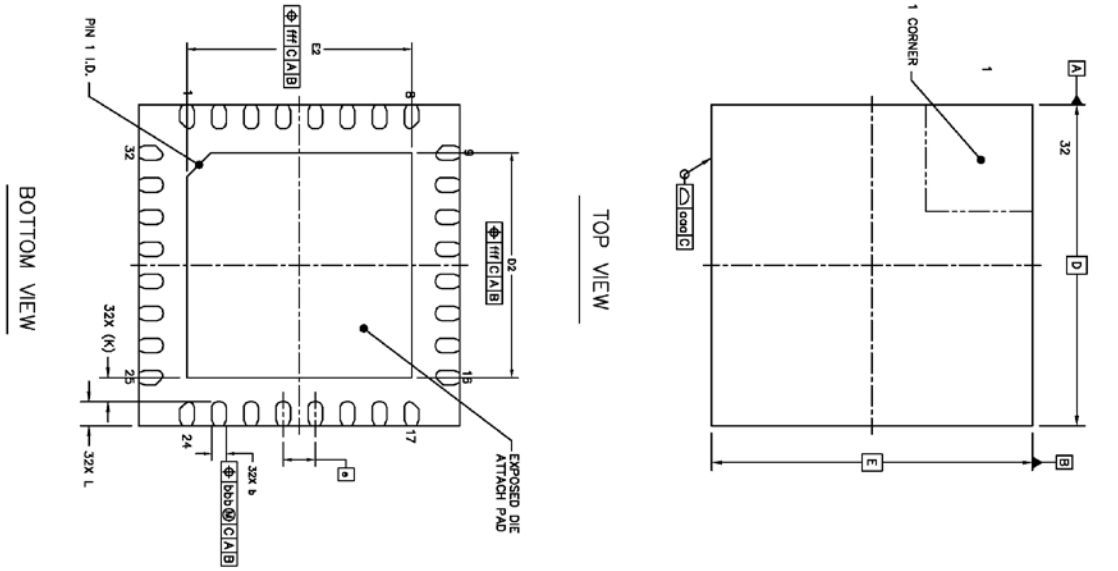


Figure 4 I²C Timing

8. PACKAGE (UNIT: MM)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		4 BSC	
BODY SIZE Y	E		4 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	D2	2.7	2.8	2.9
EP SIZE Y	E2	2.7	2.8	2.9
LEAD LENGTH	L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE	K		0.3 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.1	
EXPOSED PAD OFFSET	fff		0.1	

9. CORPORATE INFORMATION

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